

B: Amendments to The Claims:

Amend the claims to read as follows:

1 Claim 1. (Concurrently Amended) A multiprocessor computer
2 system comprising,
3 a cache coherent symmetric (SMP) computer system of
4 symmetric multiple processors having a plurality of
5 processing nodes and caches and a node controller which use
6 processor state information according to mappings provided
7 by supervisor software or firmware of allowable physical
8 processors to an application workload to determine which
9 coherent cache regions in the system are required to examine
10 a coherency transaction produced by a storage request of a
11 single originating processor of said computer system and to
12 change coherency boundaries directly with coherency mode
13 bits processor's storage request.

1 Claim 2. (Concurrently Amended) The multiprocessor computer
2 system according to claim 1 wherein a node of said plurality
3 of processing nodes of the computer has dynamic coherency
4 boundaries such that the hardware of said computer system
5 uses only a subset of the ~~total~~ processors in the said
6 computer system for a single workload at any specific point
7 in time and optimizes the cache coherency as the supervisor
8 software or firmware expands and contracts the number of
9 processors which are being used to run any single workload.

1 Claim 3. (Concurrently Amended) The multiprocessor computer
2 system according to claim 1 wherein multiple instances of a
3 physical node are connected with a second level controller
4 to create a ~~large~~ multiprocessor system having multiple node
5 controllers.

1 Claim 4. (Original) The multiprocessor computer system
2 according to claim 1 wherein said node controller uses mode
3 bits to determine which processors must receive any given
4 transaction that is received by the node controller.

1 Claim 5. (Concurrently Amended) The multiprocessor computer
2 system according to claim 1 wherein a second level
3 controller is provided which uses ~~the~~ mode bits to determine
4 which nodes must receive any given transaction that is
5 received by the second level controller.

1 Claim 6. (Concurrently Amended) The multiprocessor computer
2 system according to claim 1 wherein logical partitions are
3 provided and mapping of said logical partitions to allowable
4 physical processors is provided by ~~provided by~~ supervisor
5 software or firmware of allowable physical processors to an
6 application workload.

1 Claim 7. (Concurrently Amended) The multiprocessor computer
2 system according to claim 1 wherein logical partitions are
3 provided for the supervisor software or firmware which maps
4 allowable physical processors to an application workload and
5 a hypervisor assigns cache coherence regions which encompass
6 subsets of said ~~the total number of~~ processors and caches in
7 the system chosen for their physical proximity and defines a
8 distinct cache coherency region for each of said logical
9 partitions ~~partition~~.

1 Claim 8. (Concurrently Amended) (Concurrently Amended) The
2 multiprocessor computer system according to claim 1 wherein
3 a single workload uses only a subset of the total processors
4 in the computer system for a single workload at any specific
5 point in time for an assigned partition and a distinct cache
6 coherency ~~is optimized~~ for the address space of the assigned
7 partition as the supervisor software or firmware expands and

8 contracts the number of processors which are being used to
9 run any single workload in said assigned partition.

1 Claim 9. (Concurrently Amended) The multiprocessor computer
2 system according to claim 1 wherein a single workload uses
3 only a subset of the total processors in the computer system
4 for a single workload at any specific point in time, and
5 multiple cache coherent regions are assigned for different
6 partitions as more independent workloads coexist on ~~the same~~
7 said hardware.

1 Claim 10. (Concurrently Amended) The multiprocessor computer
2 system according to claim 1 wherein cache coherence regions
3 encompass subsets of ~~the total number of~~ processors and
4 caches in the computer system and a single workload uses
5 only a subset of the total processors in the computer system
6 for a single workload at any specific point in time for an
7 assigned partition and a distinct cache coherency ~~is~~
8 ~~optimized~~ for the address space of the assigned partition as
9 the supervisor software or firmware expands and contracts
10 the number of processors which are being used to run any
11 single workload in said assigned partition.

1 Claim 11. (Concurrently Amended) The multiprocessor computer
2 system according to claim 1 wherein software and/or firmware
3 define which subset of processors in ~~a large~~ said
4 multiprocessor must participate in a coherency transaction
5 independent of which processing node is connected to ~~the~~
6 physical DRAM storage being requested by said single
7 originating processor.

1 Claim 12. (Concurrently Amended) The multiprocessor computer
2 system according to claim 11 wherein the movement of a
3 process between nodes of ~~a large~~ said symmetric multiple
4 processors of said multiprocessor is effectuated without

5 moving physical storage contents and without requiring
6 subsequent broadcasting of the storage references originated
7 by the process from said single originating processor's
8 storage request to all of the caches in the multiprocessor.

1 Claim 13. (Currently Amended) The multiprocessor computer
2 system according to claim 1 wherein cache coherence mode
3 bits are appended to a processor's storage transactions when
4 transmitted to a connected processor of said multiprocessor
5 computer system.

1 Claim 14. (Original) The multiprocessor computer system
2 according to claim 13 wherein said cache coherence mode bits
3 are used in a decision determining whether the single
4 originating processor's storage request must be transmitted
5 to additional processors in the system.

1 Claim 15. (Concurrently Amended) The multiprocessor computer
2 system according to claim 14 wherein an increase in the
3 effective utilization of the address bandwidth of the buses
4 used to interconnect the processors of a multiprocessor
5 system allows movement of workload among physical processors
6 in a multiprocessor system at the same time as a reduction
7 of the address bandwidth required to maintain cache
8 coherency among all the processors is caused.

Claim 16. (New) The multiprocessor computer system according
to claim 1 wherein a control program for the dispatch of
virtual processors for controlling the size and extent of a
required coherency domain changes said coherency boundaries
directly with coherency mode bits.